STACKABLE LAYERS CONTAINING ENCAPSULATED INTEGRATED CIRCUIT CHIPS WITH ONE OR MORE OVERLYING INTERCONNECT LAYERS AND A ELECTRONIC PACKAGE OF MAKING THE SAME

Abstract of the Disclosure

A pre-formed integrated circuit chip is encapsulated into an electronic package, by forming an interconnect assembly separately from the pre-formed integrated circuit chip. If the interconnect assembly tests good it is bonded to the prepared integrated circuit chip. The interconnect assembly is flip bonded to the chip. The interconnect assembly and chip are passivated or potted into an integral structure to provide the electronic package. At least one test pad is defined in an interconnect layer, which test pad can be accessed and electrically connected on opposing sides of the test pad. The chip is underfilled with an insulating material to remove all voids between the chip and the interconnect assembly. The integrated circuit chip is then thinned. The test pad is accessed to test the chip. A plurality of interconnect assemblies and chips are bonded together to form a corresponding plurality of electronic packages.